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極微小デバイスへの放射線照射損傷機構の解明

2 MeV electron irradiation effect of n-SOI gate-all-around nanowire FETs

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Abstract

Input and output characteristics of n-channel SOI gate-all-around nanowire field-effect-transistors (SOI nGAANWFETs) evaluated. Device parameters as transconductance (g_m), threshold voltage (V_T), subthreshold swing (S) and drain induced barrier lowering (DIBL) are used for evaluation. The FET parameters as V_T and DIBL change suggest influence of gate shortening, but input/output characteristics do not infer remarkable. After the 2 MeV electron irradiation, drain current (I_D) decreased. Degree of I_D degradation by 2 MeV electron irradiation evaluated using gm and S, these are differed by gate width and length of the device. The gm and S degradation for a wide device of the gate width was remarkable. It can be concluded that when the device size became small, radiation tolerance increased, because of influence from buried oxide layer which lied under the nanowire-gate degradation by 2 MeV electron irradiation.

Keyword: Gate-all-around FET, electron irradiation, radiation tolerance

1. Introduction

Multiple gate devices were considered as an alternative for planar complementary metal oxide semiconductor (CMOS) scaling [1]. FinFET is a most popular structure, which have a fin-gate structure have shown superior short-channel effect control [1, 2]. Nowadays, for 28 nm and below CMOS technologies there is a competition between planar fully depleted Silicon-on-Insulator (SOI) devices and FinFETs. FinFETs can be fabricated on either bulk silicon or SOI substrates. After a decade of extensive research with the efforts to improve and study the device performance, the main semiconductor industries have been investing in this technology. Apart from FinFET structures, various structures and/or materials have been demonstrated for the 20-nm node and beyond. Ultra-thin body and buried oxide (BOX) and gate-all-around (GAA) devices with the gate fully wrapped around the device body promising candidates for the next generation technology nodes. The BOX, such as FD SOI has significantly improved the threshold voltage (V_T) variability and minimizing the short-channel effect [3].

The scaling of CMOS technologies leads to an intrinsic hardening against certain radiation effects, like Total Ionising Dose (TID) damage, so that the implementation of commercial-of-the-shelf ULSI components and circuits for harsh environments is becoming more popular [4-6]. This has been driven by multiple factors, including the implementation of microelectronics components and circuits in nuclear plants, high energy particle accelerators and artificial satellites. At the same time, this can eliminate the possible impact of radiation-induced trapped charges in the BOX layer or at the Si/BOX interface, so that high total-dose hardness is anticipated [7].

In this study, an electric characteristic of the SOI nGAA nanowire (NW) FETs such as short channel effect by reduction of device scales and degradation of input and output characteristics before and after irradiated 2 MeV electrons are investigated. Especially, radiation tolerance compared to the attention of gate width and length.

2. Experimental Mechod

Figure 1 shows a studied device structure of a SOI n-channel GAANWFET [8]. Devices were processed on SOI substrates. For junction less devices, channel doping was obtained via ion implantation. This was followed by a spike anneal, after which device processing continued according to the baseline flow sequence dummy-gate electrode deposition (a-Si). The gate stack used in all devices was obtained by a replacement Metal Gate (RMG) high-k process and it consists of: an interfacial layer-SiO_2 formed by O_3-oxidation and a high-k dielectric (HfO_2) grown by atomic layer deposition, followed by the effective work function-metal and tungsten as the fill-metal. S/D silicide was done after the RMG module by opening vias through the stack, landing on the S/D areas. The device parameters of gate lengths (L) and widths (W) are listed in Table 1.

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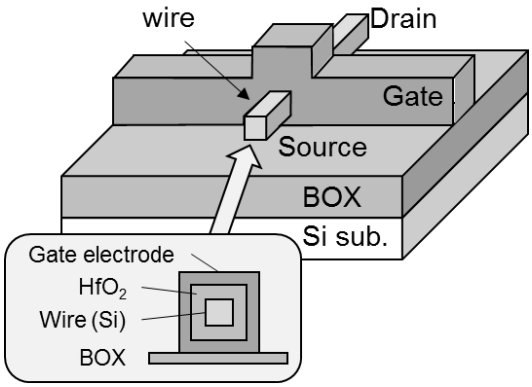

Figure 1. Device structure of the SOI nGAANWFET. Nano wire is surrounded by gate electrode.

In this study, damage of the electrical properties by 2 MeV electrons irradiation of SOI nGAANWFETs is investigated. Devices without applied bias voltage were irradiated at room temperature by 2 MeV electrons in the electron accelerator at the Takasaki QST. The electron fluence varied from 1×10^{14} to 1×10^{16} e/cm^2. Input and output characteristics of SOI nGANWFET were measured before and after the 2 MeV electron irradiation using Keysight Technology B1500A device parameter analyzer.

Table 1. The list of gate length and width of the SOI nGAANWFETs.

Device #	*gate length L (nm)*	*gate width W (nm)*	*L/W*
E24T7	250	1000	0.25
E24T8	450	1000	0.45
E24T9	1000	1000	1.0
E23T9	1000	130	7.8
E22T10	1000	40	25

3. Results and Discussion

Figure 2 shows the input characteristics of the devices of E24T7 (L and W = 0.25 and 1.0 μm) and E24T9 (L=1.0/W=1.0 μm) before and after the 2 MeV electron irradiation (1×10^{16} e/cm^2). The drain current (I_D) increased and VT shifts negative by gate length shorting. After the electron irradiation, it can be confirmed that I_D decrease and V_T negative shift. These electrical properties change by electron irradiation are smaller than general planer FETs [9].

Electrical characteristics of SOI nGAANWFETs for before irradiation were studied. Figure 3 shows transconductance (g_m) of the devices against with the gate length and width (L/W) ratio. There are some combination of L and W for used device, to arrange with conductance of device from low one to high one, the L/W

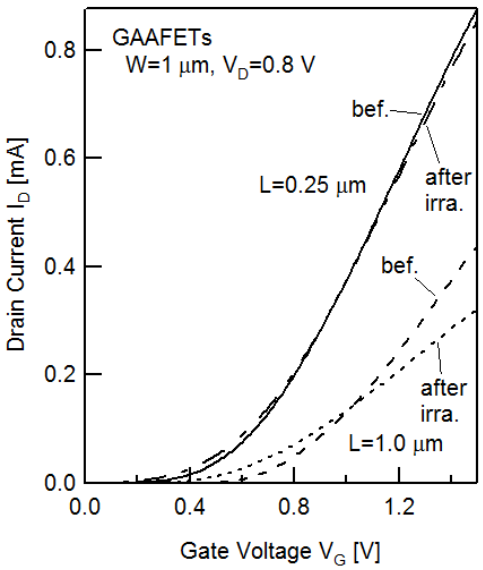

Figure 2. Input characteristics of the SOI nGAANWFETs before and after 2 MeV electron irradiation (1×10^{16} e/cm^2). Gate length is L = 0.25 and 1.0 μm.

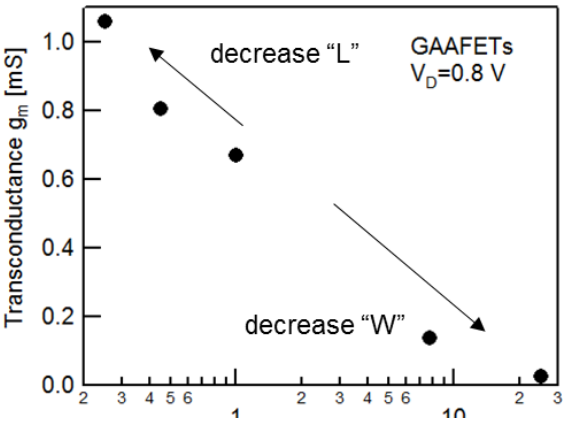

Figure 2. Transconductance of the SOI nGAANWFETs as a function of L/W ratio.

ratio introduce for evaluation. Correspondence of device number and L/W ratio listed in Table 1. In the case of L/W=1, it is largest device of our use (E24T9, L=1.0/W=1.0 μm). When gate length decrease, the gm goes to the left side, and when gate width decrease, the gm goes to the right side. From Fig. 3, it can be said that gm change simply corresponds to the physical structure of gate. On the other hand, the short channel effect is concerned for the FETs which gate length became short. To evaluate this problem, V_T and drain induced barrier lowering (DIBL) which determined by eq. (1) [10],

$$\mathrm{DIBL} = \frac{V_T(V_D=0.1\ V)-V_T(V_D=0.8\ V)}{0.8\ V-0.1\ V} \qquad (1),$$

plotted with L/W ratio are shown in Figure 4. When the L becomes short, the L/W increase, and the V_T decreased and the DIBL increased. These suggest that short channel effect revealed with short L devices. However, drain current of output characteristics influence of short channel effect to the device operation seems small. Figure 5 compare output characteristics of the devices of short L (E24T7, L=0.25 μm) and long L (E24T9, L=1.0 μm). Both of I_D for saturation region slightly increased with increase of V_D. Compare with both characteristics, it can be say that no remarkable increase of slope at saturation region. In this case, device scale down is no significant inferred to the short channel effect of SOI nGAANWFETs.

Next, electrical characteristics degradation of the SIO nGAANWFETs by 2 MeV electrons discussed. As shown in Fig. 2, it is no significant decrease of I_D for E24T7 after 1×10^{16} e/cm^2 electron irradiation, while I_D for E24T9 decreased. It seems that the FETs in short gate length are higher radiation gm than that of long one. To

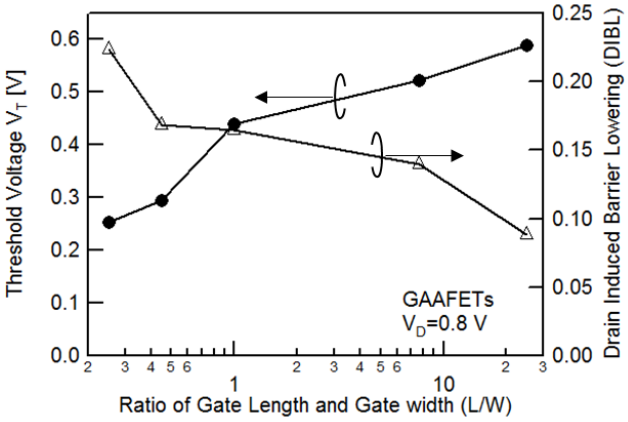

Figure 4. Device structure (L/W) dependence of threshold voltage (V_T) and drain induced barrier lowering (DIBL) before 2 MeV electron irradiation.

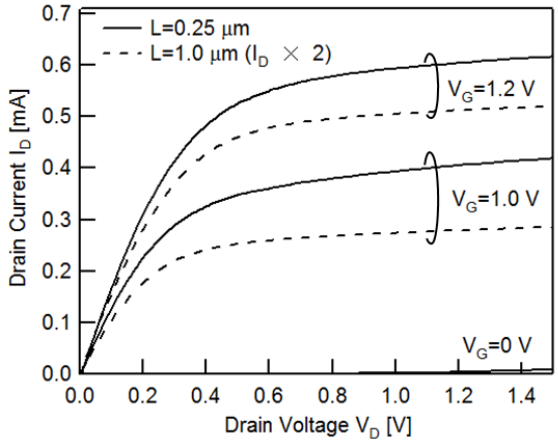

Figure 5. Output characteristics of the SOI nGAANWFETs for gate length of L = 0.25 and 1.0 μm.

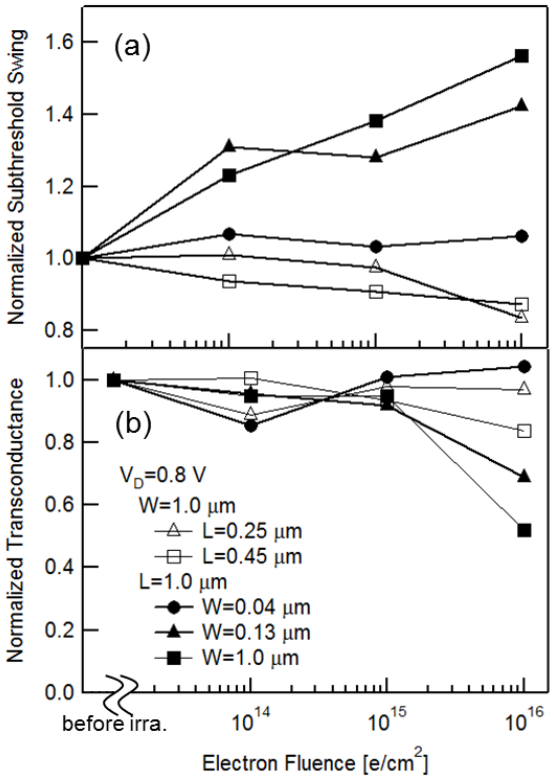

Figure 6. Subthreshold swings (a) and transconductances (b) of the SOI nGAANWFETs as a function of 2 MeV electron fluence. These are normalized using the value of before irradiation.

compare I_D degradation degree by electron irradiation with the parameter of gate width and lengths subthreshold swings (S) and g_ms normalized by the value of before electron irradiation are shown in Figure 6. For the devices of L=0.25 μm which is shorter one and of W=0.04 μm narrower one, S and gm do not change largely at 1×10^{16} e/cm^2 electron irradiation. In contrast, gm changes remarkable, when L and W becomes long and wide, respectively. For the L=1.0/W=1.0 μm device, gm was decreased 50% compared to before irradiation. It pays attention to device structure, differences of radiation tolerance were considered. The nanowire gate which surrounded gate oxide fabricated on the BOX. It had been reported about subthreshold swing inferred by charge accumulation of BOX layer and it changes gate width [11]. Also, it is well known that charges accumulated in the oxide bulk and interface by radiation, and it inferred input and output characteristics of FET [12, 13]. In this case, influence of electron irradiation induced charge at BOX to the wider gate device larger than that of narrower one.

Figure 7 shows the output characteristics of 1×10^{16} e/cm^2 electron irradiated nGAANWFETs. For the device of L=1.0 μm, gm and DIBL degraded by electron irradiation, though slope of saturation region does not

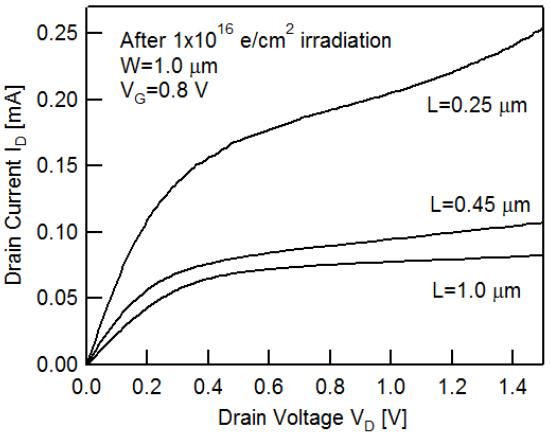

Figure 7. Output characteristics of the SOI nGAANWFETs after 2 MeV electron irradiation (1×10^{16} e/cm^2). Gate widths are fixed W=1.0 μm, and gate lengths are L = 0.25, 0.45 and 1.0 μm.

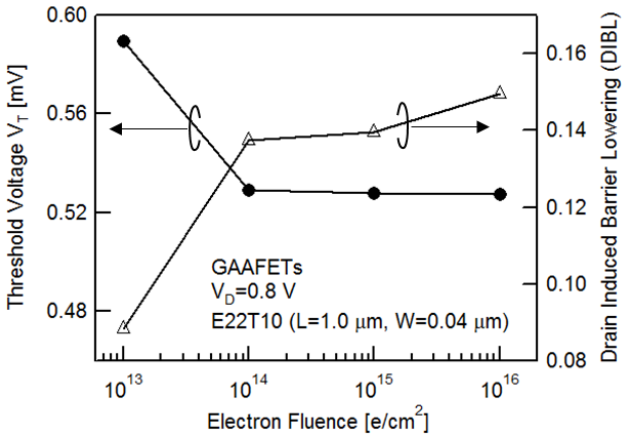

Figure 8. Threshold voltage (V_T) and drain induced barrier lowering (DIBL) changes for the device of E22T10 (W=1.0/L=0.25 μm) before and after 2 MeV electron irradiation.

increase largely. In contrast, for the device of L=0.25 μm, saturation region of output characteristic slope rises. Also, V_T decreased and DIBL increased by electron irradiation as shown in Fig. 8. As discussed above, short channel effects of nGAANWFET are emphasized by electron irradiation.

4. Conclusion

2 MeV electron irradiation influences of input and output characteristics for the n-channel SOI gate-all-around FETs were investigated. Device parameters of V_T, gm, DIBL tendency are lined up by the ratio of gate length and gate width (L/W). There are no serious problems to the input and output characteristics by device size reduction as short channel effect. Radiation tolerance of the devices as a function of the gate size to the irradiation of 2 MeV electrons compared. It was revealed that radiation tolerance was high so that device size became small. Transconductance and subthreshold swing do not degrade even electron fluence increased to 1×10^{16} e/cm^2, while transconductance about 50 % decreased when the gate width became wider. The main degradation factor is considered by charge accumulation to the buried oxide under the nanowire-gate by electron irradiation. It can be concluded that the objected device which especially device size became small, has high radiation tolerance.

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